LDMOS Transistors in Power Microwave Applications

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***Abstract*— LDMOS transistors have become the device choice for microwave applications. An overview is given of the LDMOS technology improvements at 3.6 GHz over the last decade, and RF performance of LDMOS microwave products for S-band radar is presented.**

I. Introduction

More than ten years ago LDMOS transistors were introduced as a replacement of bipolar transistors for RF power applications [1,2]. Nowadays LDMOS technology is the leading RF power technology for base station applications, in particular for GSM-EDGE applications at 1 and 2 GHz, WCDMA applications at 2.2 GHz and more recently for WiMax applications around 2.7 GHz and 3.8 GHz.

One of the last niche application areas in which bipolar devices were used was the 3-4 GHz microwave area, such as S-band radar. Main reason for this was that earlier generations of LDMOS showed a similar performance at 3 GHz compared to bipolar, which did not justify redesign of complex radar systems.

The main driver for LDMOS is a high volume application, which enables continuous improvement of the LDMOS technology [3,4], and this has resulted in the latest generation LDMOS, which outperforms bipolar at S-band frequencies with some additional advantages such as ruggedness and better thermal behaviour. In this article an overview is given of the LDMOS improvements at 3-4 GHz and the LDMOS performance for microwave products is presented.

II. LDMOS Advantages

LDMOS transistors are voltage-controlled devices, so no gate current is flowing as in bipolar devices. This voltage control allows a much simpler and cheaper bias circuitry compared to bipolar devices. The drawback of a weak gate-oxide does no longer hold, since nowadays ESD devices are standard.

Another advantage is the source connection to the bulk-backside of LDMOS, while bipolar devices have a collector back side. Therefore bipolar uses isolating BeO packages in combination with bond wires. LDMOS allows for a replacement of the toxic BeO packages by environment friendly ceramic or plastic packages. This is a major advantage for LDMOS. A picture of such a ceramic SOT502 packages is shown in Fig. 1. Internal input and output (inshin) matching is provided within the package to transform the impedance levels and reduce RF losses. The bulk source is eutectically soldered to the package without the need for source bond wires. Without the source wires LDMOS does not have the additional source inductance resulting in a high gain of the LDMOS power transistor.

LDMOS also has a better temperature stability than bipolar. Bipolar devices have a positive temperature coefficient leading to thermal runaway. Bipolar therefore needs elaborate temperature compensation like ballast resistors to protect the device against failures. At high current, LDMOS has a negative temperature coefficient automatically turning off the device when fully powered. This leads to a natural advantage with respect to thermal properties and ruggedness.

LDMOS devices have high flexibility with respect to pulse duration, as is important for microwave applications. The common source configuration of LDMOS stabilizes the device and prevents oscillations at lower pulse durations.

The RF performance of LDMOS at 3-4 GHz frequencies has also dramatically improved in the last decade to become significantly better than bipolar performance. In section IV the LDMOS RF performance is shown for 3.6 GHz, but first state of the art LDMOS technology is described in section III.

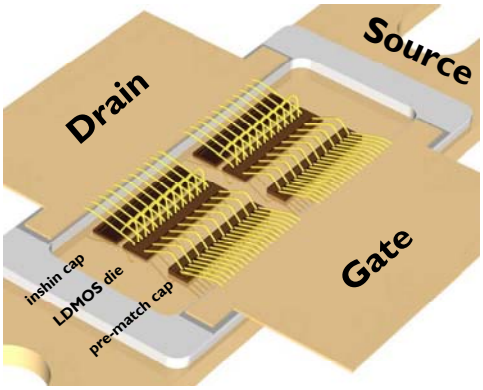

Figure 1: Picture of LDMOS devices in a ceramic package with internal pre and post matching.

III. LDMOS Technology Evolution

The LDMOS technology of NXP is processed in an 8-inch CMOS-fab capable of lithography down to 0.14 um, where the LDMOS process is derived from C075 CMOS (0.35um gate) process. Additions to the C075 process are LOCOS isolation, the source sinker to the substrate, back-side metallization, CoSi2 gate silicidation, tungsten shield, mushroom-type drain structure with thick 5 layer AlCu metallization.

A schematic cross-section of LDMOS is shown in Fig. 2. The LDMOS n+ source region is connected to the backside via a metal bridge, a p+ sinker, and a highly conducting p+ substrate. Current will flow from source to drain if the gate is positively biased inverting the laterally diffused p-well.

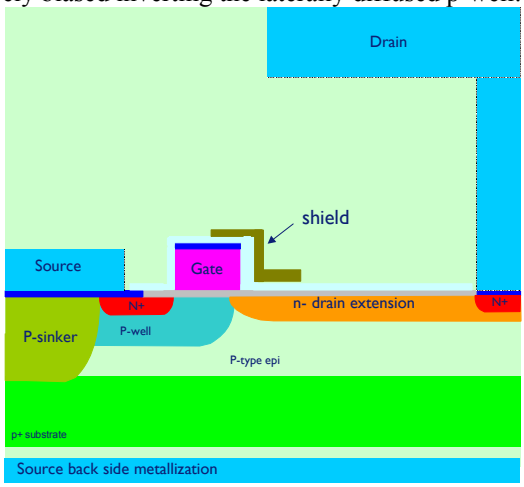

Figure 2: Schematic cross-section of state of art RF LDMOST fabricated in an 8 inch CMOS fab.

The LDMOS further consists of a drain extension area to realize a breakdown voltage of more than 65V, and multi layer drain metallization to give excellent electromigration properties. The drain is shielded from the gate by a tungsten field plate realizing an extremely low feedback capacitance and good hot carrier reliability properties. Many fingers are placed in parallel to form a power die, resulting in a total finger length of 10-100 millimeters.

IV. LDMOS Performance Evolution at 3.6 GHz

We show LDMOS devices measured at 3.6 GHz with a load-pull set-up in a water-cooled test circuit. The devices have a power level of 10-20 W to allow low Q matching with the load pull tuners and measure the intrinsic device performance evolution. All devices are biased with a supply voltage of 28V and a drain current of 5 mA per mm finger length to achieve class AB performance.

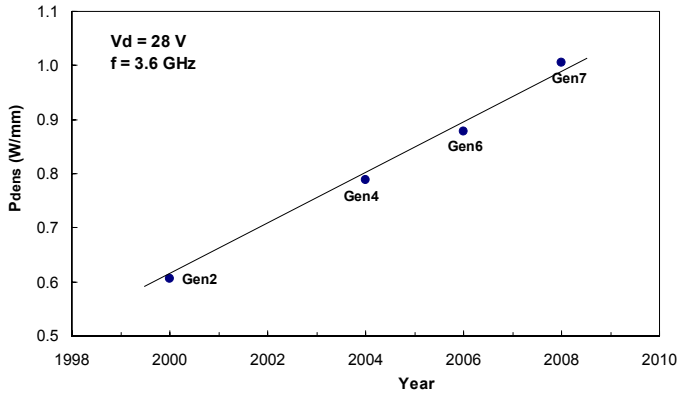

Figure 3: Evolution of the LDMOS power density at 3.6 GHz measured for packaged devices without internal matching in a load pull set-up.

The evolution of power density (3dB compression power) is shown in Fig. 3. Over the last decade the power density has about doubled, achieving more than 1 W/mm for the 7th generation of NXP LDMOS. Especially for microwave applications there is a continuous demand for higher power. The gain evolution at 3.6 GHz is shown in Fig. 4. The gain has increased from 7dB in the year 2000 to 14dB for the most recent technology generation. Bipolar devices have at this frequency a gain of about 9dB, a similar performance to the first few LDMOS generations, not justifying a redesign of complex radar systems. However the 14dB gain of the later generations is 5dB in excess of bipolar technology, and explains designing-in LDMOS technology.

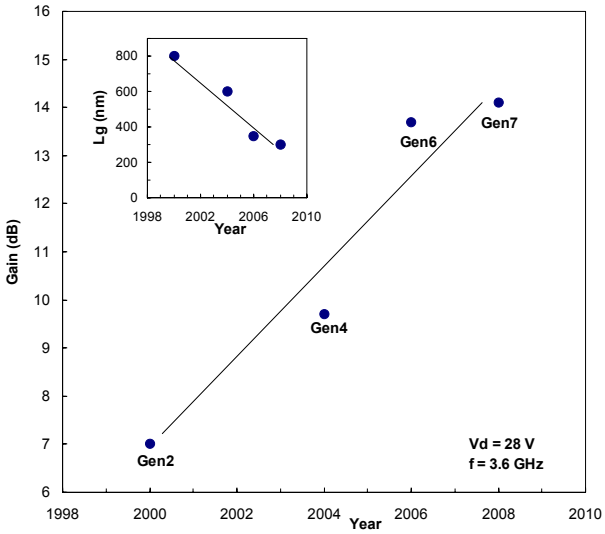

Figure 4: Gain improvement at f=3.6 GHz for the subsequent LDMOS generations as measured by load pull techniques. The inset shows the reduction of the gate length.

In the inset of Fig. 4 we have plotted the reduction of gate length for the subsequent generations. The gate length has been dramatically reduced to increase the gain of the transistor via an increase of the transconductance. Now other contributions, like input capacitance, feedback capacitance and source inductance become of importance. LDMOS leverages the advantage of a low source inductance as a consequence of the backside source connection (opposing the bond wires for bipolar devices) and the low feedback capacitance due to the shielding construction.

The evolution of drain efficiency at 3.6 GHz is plotted in Fig. 5. The peak efficiency of the latest generation LDMOS is about 55%, while the maximum theoretical class AB efficiency is 78.5%. The theoretical efficiency is approached at frequencies below 1 GHz, indicating that frequency dependent losses limit the efficiency at 3.6 GHz [3]. The evolution of peak efficiency has mainly been achieved by a reduction of the output capacitance losses. This output capacitance reduction has been plotted in Fig. 6. The output capacitance has been reduced by a factor 2 in the last decade.

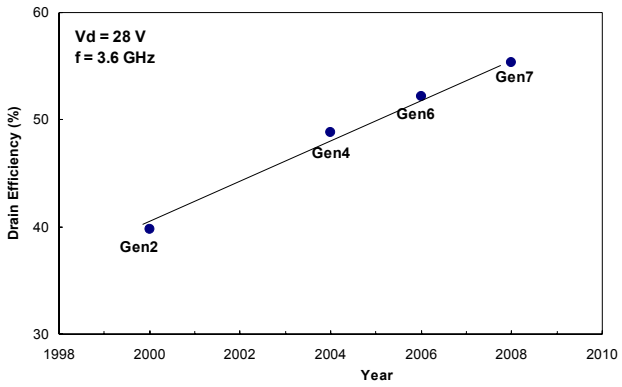

Figure 5: Evolution of LDMOS peak drain efficiency at 3.6 GHz for a supply voltage of 28 V.

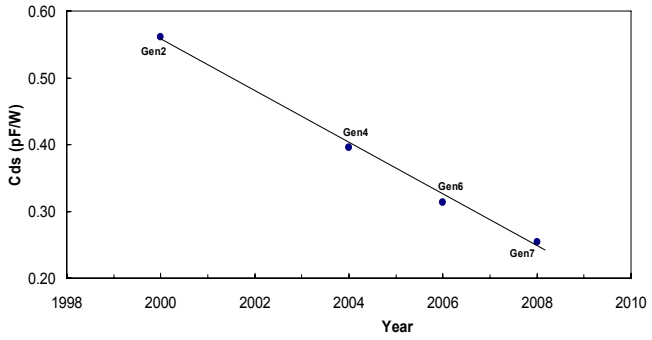

Figure 6: Reduction of off-state output capacitance at Vd = 28V for subsequent LDMOS generations.

This LDMOS evolution of power density, gain and efficiency, fuelled by the high volume base station market, has resulted in an extension of the application area of LDMOS. The WiMax [4] and microwave markets nowadays widely use LDMOS technology.

IV. LDMOS Reliability

The LDMOS process qualification is derived from the CMOS standard procedures as used by NXP Semiconductors [5], which comply with the standards of industry. Special attention is paid to the hot carrier degradation: electrons and holes are trapped in the surface oxide due to the high electric fields in combination with high current densities during operation. The degradation is measured for a transistor at bias conditions, which is typically at a current of 5mA per mm gate width and a drain-source voltage of 28V. A degradation of bias current, maximum current or on-resistance could lead to a change in device performance. In Fig. 7 we have plotted the Idq degradation for the subsequent LDMOS generations. The degradation has been reduced over the years and has now arrived at a low level of less than 5% degradation after an extrapolation to 20 years.

Furthermore we have extensively tested the LDMOS for electromigration. The latest generations use wide and thick mushroom-shape multi-layer AlCu metallization. The electromigration MTF numbers for these stacks are superior compared to the 2-layer Au metallization stack used in the earliest LDMOS generations.

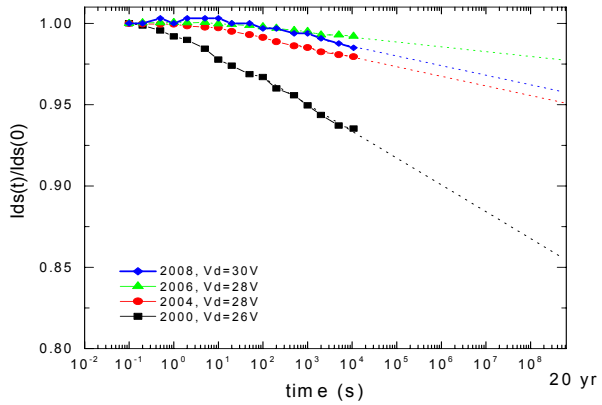

Figure 7: Degradation of the bias current as a function of time at room temperature. The LDMOS is biased at 26-30 V and a quiescent current of 5 mA/mm.

V. LDMOS Microwave Product Performance

The continuous technology improvement has generated best in class microwave products. This is demonstrated in Fig. 8 for 100W broadband matched devices in the range 2.7-3.1 GHz. The gain is plotted for a Gen6 LDMOS device (BLS6G2731-120), a Gen4 LMDOS device (BLS4G2731-100), and a bipolar device (BLS2731-110). Where the Gen4 device only has 0.5dB higher gain than the bipolar device, the Gen6 device outperforms the bipolar device by more than 5dB.

Furthermore the Gen6 LDMOS device has 10W more power and higher drain efficiency over the band. This is illustrated in Fig. 9. Clearly a 5-10% surplus of drain efficiency compared to bipolar technology has been achieved.

Another LDMOS microwave product is the BLS6G3135-120 for S-band applications in the frequency-range 3.1-3.5 GHz. The gain and efficiency of this 120W microwave product is plotted in Fig. 10.

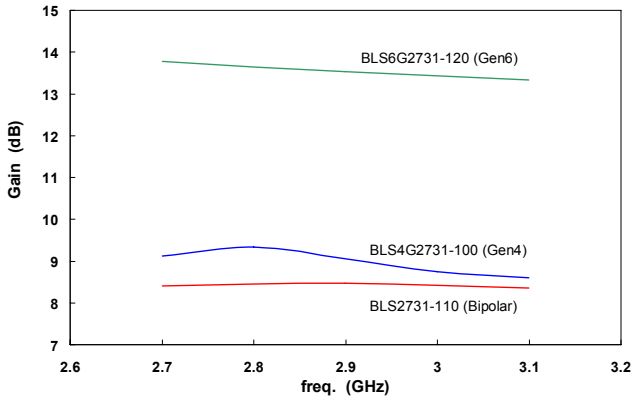

Figure 8: Gain comparison of broadband matched devices operating in the 2.7-3.1 GHz frequency band.

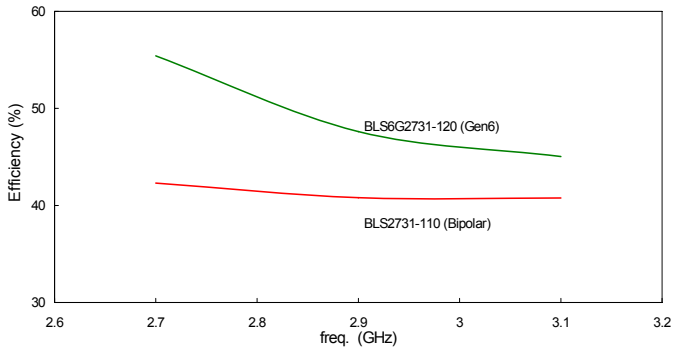

Figure 9: Drain efficiency comparison of broadband matched devices operating in the 2.7-3.1 GHz frequency band.

The BLS6G3135-120 clearly shows a considerably better gain and efficiency compared to state of the art bipolar products. At 3.1 GHz the efficiency is close to 50% and at the high end of the frequency band, due to the broadband matching of the device, still approximately 44% has been achieved. The broadband gain is 11-12dB.

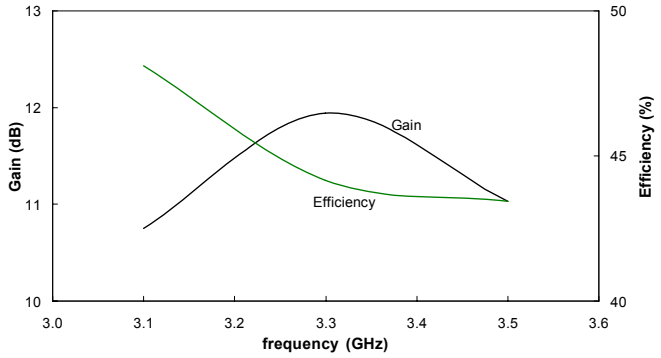

Figure 10: Gain and efficiency of the BLS6G3135-120.

VI. Microwave Product Reliability

The thermal impedance (Z_{TH}) of the LDMOS products is significantly better than their bipolar counterparts. For example the bipolar MX0912B251Y has a Z_{TH} of 0.28 K/W when operating at a pulse length of 10 µs and a duty cycle of 10%, while the Gen 2 LDMOS equivalent BLA0912-250 has a Z_{TH} of 0.13 K/W under identical conditions.

Furthermore the efficiency of LDMOS devices is higher as shown in the previous paragraph. The combination of the low Z_{TH} and high efficiency results in a much lower junction temperature for LDMOS and a better reliability.

This lower junction temperature in combination with the negative temperature coefficient of MOS devices has a positive effect on the overdrive capability of LDMOS products. The overdrive capability of the BLS6G3135-120 is shown in Fig. 11. This device easily tolerates 5dB overdrive without device degradation.

NXP microwave products can withstand large VSWR mismatch conditions and make use of a specially optimized LDMOS process for pulse shaped signals. Given the importance of this topic, we will elaborate on the ruggedness improvements in a separate publication.

In (phased array) radar applications, where a large number of amplifiers are combined, the insertion phase becomes an important parameter.

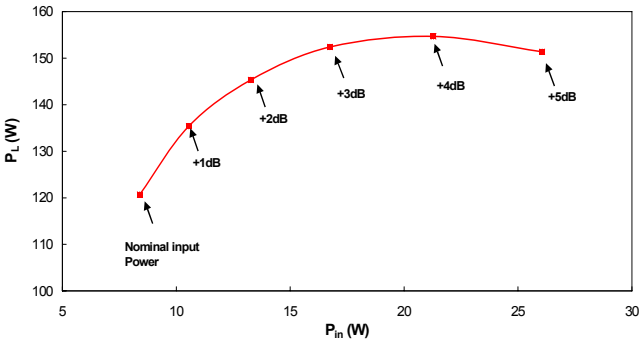

Figure 11: BLS6G3135-120 overdrive capability measured at 3.5 GHz, Vds = 32 V, Idq = 100 mA, tP = 300µs, δ = 10%.

The common source configuration of LDMOS reduces the coupling between the different bond-wires in the internal matching circuit. This configuration in combination with the CMOS process control improves the spread in insertion phase, as can be seen from Fig. 12. In this figure the normalized insertion phase from a large number of different assembly and diffusion batches is plotted. LDMOS clearly shows a much narrower distribution compared to bipolar.

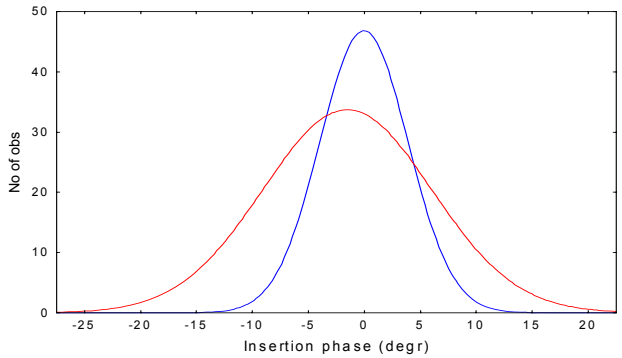

Figure 12: Batch to batch insertion phase distribution of both LDMOS and bipolar devices at S-Band frequencies.

VII. RF Power Technology Overview

During the last decade LDMOS technology has rapidly evolved in performance becoming the preferred technology for RF power transistors. In this article we have focussed on the replacement of bipolar devices by LDMOS technology in microwave applications and we have explained the advantages of LDMOS. LDMOS is nowadays the technology of choice for design-ins in base station, broadcast, ISM, and microwave applications. GaAs technology is hardly used for these applications, but is preferred for 4W mobile phone amplifiers. For lower power levels (below 1W) the market is dominated by CMOS. New technologies are continuously evolving but have not yet matured as RF power technology, where

reliability is an important criterion. GaN now has taken over from SiC the role of most promising (but still immature) technology of the future for high frequency, high power applications. Such a technology could open the realization of more advanced concepts like switch mode power amplifiers. NXP heavily invests in advanced concept research being a top European GaN player. An overview of preferred technologies for today's design-ins as a function of power and frequency is given in Fig. 13. We see than LDMOS is expanding towards the high frequency (>3.5 GHz) applications and towards high power applications. LDMOS has occupied a solid position as RF Power technology with the prospect of developing into more and new applications.

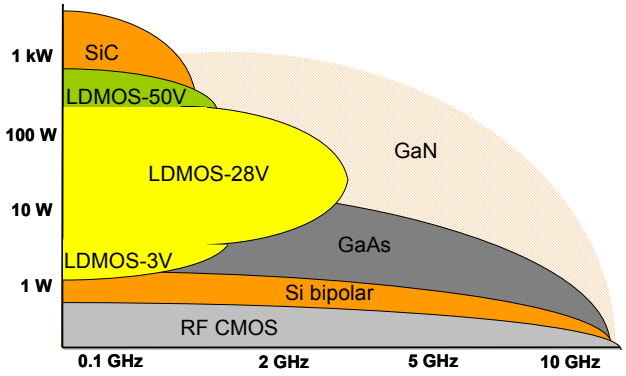

Figure 13: An overview of preferred transistor technologies for design-ins in the year 2008 as a function of power and frequency. LDMOS is continuously expanding towards higher power and frequency.

VIII. Conclusions

To conclude we have shown an overview of the LDMOS technology improvements at 3.6 GHz over the last decade. LDMOS technology has become the device choice for microwave applications. The presented LDMOS microwave products for S-band radar easily outperforms bipolar products, while having additional advantages as better ruggedness and thermal properties.

Acknowledgements

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